| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
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| **Date of Performance:** | **18 / 07 / 2023** | **Batch No:** | **C-1** |
| **Faculty Name:** |  | **Roll No:** | **16010122257** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 1**

**Title: Study of Basic Gates and Universal Gates**

| **Aim and Objective of the Experiment:** |
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| Understand Basic Logic Gates and Universal Gates |

| **COs to be achieved:** |
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| **CO1**: Recall basic gates & logic families and binary, octal & hexadecimal calculations and conversions. |

| **Tools used:** |
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| Trainer kits |

| **Theory:** |
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| Logic gates are electronic circuits that perform logical operations on one or more input signals to produce an output signal based on a set of logical rules. Logic gates can be classified into the following categories:   1. Basic Gates:    1. AND Gate: The AND gate produces a high output (1) only when all of its inputs are high (1).    2. OR Gate: The OR gate produces a high output (1) if any of its inputs is high (1).    3. NOT Gate (Inverter): The NOT gate produces the logical complement of its input. It takes a single input and produces the opposite value as the output. 2. Derived Gates:    1. NAND Gate: The NAND gate is a combination of an AND gate followed by a NOT gate. It produces the inverse of the AND gate's output. It outputs a low (0) only when all of its inputs are high (1).    2. NOR Gate: The NOR gate is a combination of an OR gate followed by a NOT gate. It produces the inverse of the OR gate's output. It outputs a high (1) only when all of its inputs are low (0).    3. XOR Gate (Exclusive OR): The XOR gate produces a high output (1) when the number of high inputs is odd. It outputs a low (0) when the number of high inputs is even.    4. XNOR Gate (Exclusive NOR): The XNOR gate produces a high output (1) when the number of high inputs is even. It outputs a low (0) when the number of high inputs is odd. 3. Universal Gates:   NAND and NOR gates are considered universal gates because any logic function can be implemented using only NAND gates or only NOR gates. This means that with a sufficient number of NAND or NOR gates, you can create circuits that can perform any logical operation. |

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| **Implementation Details** |

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| |  |  | | --- | --- | | AND Gate:Y=  Symbol  Pin diagram    Truth Table: | WhatsApp Image 2023-08-04 at 21.45.05.jpeg |  |  |  | | --- | --- | | OR Gate: Y =    Symbol  Pin Diagram      Truth Table: | WhatsApp Image 2023-08-04 at 21.45.06.jpeg | | WhatsApp Image 2023-08-04 at 21.45.06 (1).jpeg |  |  |  | | --- | --- | | NOT Gate: Y =  Symbol  Pin Diagram  Truth Table: | WhatsApp Image 2023-08-04 at 21.45.06 (2).jpeg |  |  |  | | --- | --- | | NAND Gate: Y =  Symbol  Pin Diagram  Truth Table: | WhatsApp Image 2023-08-06 at 12.40.43.jpeg |  |  |  | | --- | --- | | NOR Gate: Y =  Symbol  Pin Diagram  Truth Table: | WhatsApp Image 2023-08-06 at 12.40.44.jpeg |  |  |  | | --- | --- | | XOR Gate: Y =      Symbol | WhatsApp Image 2023-08-06 at 12.40.44 (1).jpeg | | Pin Diagram | WhatsApp Image 2023-08-06 at 12.40.45 (2).jpeg | | Truth Table: | WhatsApp Image 2023-08-06 at 12.40.45.jpeg |  |  |  | | --- | --- | | XNOR Gate: Y =    Symbol | WhatsApp Image 2023-08-06 at 12.40.44 (2).jpeg | | Pin Diagram | WhatsApp Image 2023-08-06 at 12.40.45 (3).jpeg | | Truth Table: | WhatsApp Image 2023-08-06 at 12.40.45 (1).jpeg |  |  |  | | --- | --- | | **Implementation Using NAND Gate**  **NOT GATE**  **AND GATE**  **OR GATE** | WhatsApp Image 2023-08-06 at 13.05.35.jpeg |   **Implementation Using NOR Gate**   |  |  | | --- | --- | | **NOT GATE** | WhatsApp Image 2023-08-06 at 13.05.35 (1).jpeg | | **AND GATE** | WhatsApp Image 2023-08-06 at 13.05.36.jpeg | | **OR GATE** | WhatsApp Image 2023-08-06 at 13.05.35 (2).jpeg | |

| **Post Lab Subjective/Objective type Questions:** |
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| 1. Implement the Boolean function using NAND gates and NOR gates F=A’B + AB’   WhatsApp Image 2023-08-04 at 21.45.07.jpeg  WhatsApp Image 2023-08-06 at 22.36.34.jpeg   1. Implement using combination of gates F = ABC + AB’C + ABC’   WhatsApp Image 2023-08-04 at 21.45.07 (1).jpeg  WhatsApp Image 2023-08-04 at 21.45.07 (2).jpeg |

| **Conclusion:** |
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| WhatsApp Image 2023-08-04 at 21.45.08.jpeg  WhatsApp Image 2023-08-04 at 21.45.08 (1).jpeg |

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| **Signature of faculty in-charge with Date:** |